VERSION WITH MARKINGS TO SHOW CHANGES MADE

TITLE:

Specification at page 1, line 1:

~~MULTILAYER CERAMIC SUBSTRATE AND METHOD FOR FABRICATING THE SAME~~METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE

SPECIFICATION:

Specification at page 1, line 5:

CROSS-RELATED APPLICATIONS

This application is a Divisional application of U.S. Patent Application Serial No. 09/173,288, filed October 14, 1998.

CLAIMS:

15. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein a meshed pattern is provided in a part of said conductive pattern.

16. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein a shield pattern is provided at an outer edge of said conductive pattern.

17. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

18. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising a dielectric layer formed on a part of said ceramic substrate.

19. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

20. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip

21. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or claim 14], further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

Claims 1-12 have been cancelled.

Claims 22-28 are newly added.